

IMPROVED FERROELECTRIC MEMORY ARCHITECTURE

Abstract of Disclosure

An improved architecture which reduces the adverse impact of the disturb pulse on non-selected ferroelectric memory cells is disclosed. The architecture provides plateline selection switches for selectively coupling memory groups on the selected side of the memory block to the plateline and decoupling the non-selected side of the memory block from the plateline. By decoupling the non-selected side of the memory block from the plateline, the plate pulse does not adversely affect the memory cells in the non-selected side of the memory block.